REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 31, 34-38 and 43-65 are pending in the application. The Examiner additionally stated that claims 31, 34-38 and 43-65 are rejected. By this amendment, claims 37 and 50-65 have been cancelled and claims 31, 34, and 38 have been amended. Hence, claims 31, 34-36, 38 and 43-49 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §112

The Examiner rejected claim 31 under 35 U.S.C. 112, second paragraph as lacking sufficient antecedent basis. Applicant has amended claim 31 to provide sufficient antecedent basis.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 31, 43-44, and 46-49 under 35 U.S.C. 103(a) as being unpatentable over Narayan et al., U.S. Patent No. 5,850,532 (hereinafter *Narayan*) in view of Hoyt et al., U.S. Patent No. 5,604,877 (hereinafter *Hoyt*). Applicant respectfully traverses the Examiner's rejections.

Narayan discloses a microprocessor that includes a prefetch/predecode unit that fetches instructions from main memory and stores the fetched instructions into an instruction cache. During this process, the predecode unit decodes the incoming bytes and generates predecode bits that are stored into the instruction cache along with the instruction bytes. The predecode bits include a start bit to indicate whether the byte is the start byte of an instruction, an end bit to indicate the end byte of an instruction, and a functional bit. The

functional bit is set if the byte is a prefix byte of the instruction according to the x86 instruction set and is clear for non-prefix bytes (indicated by col. 7, lines 10-21; Applicant notes there appears to be an inconsistency in the polarity of the bits indicated at col. 7, lines 4-5). Consequently, by examining the functional bits for an instruction, decode units may subsequently determine that the instruction byte associated with the first clear functional bit is the opcode byte of the instruction. Additionally, the functional bits may be used to indicate whether an instruction is an MROM instruction (complex instruction requiring microcode sequence generation) or is of the fast path type that can be directly decoded.

The microprocessor of *Narayan* also includes a scanning unit that receives the predecode bits when a cache line of instruction bytes is fetched from the instruction cache. The scanning unit scans the predecode data to locate the beginning and end of each instruction. The scanning unit efficiently processes the predecode data in order to identify instructions to select for dispatching into the instruction processing pipeline. In parallel, the scanning unit scans the predecode data to detect whether the predecode data is valid. In particular, an invalid instruction scan unit scans the predecode bits to detect whether the predecode bits are invalid, which may occur, for example, if a program included a branch instruction that branched to a target address at which the opcode of an instruction is stored, thereby bypassing any prefix bytes for the instruction. See col. 15, line 65 to col. 16, line 6.

Notably, Applicant can find no teaching in *Narayan* of the functional bits indicating that *Narayan*'s branch prediction unit predicted a byte is an opcode byte of an instruction in an instruction buffer. Rather, the predecode unit generates the functional bits. *Narayan* does state that the predecode unit may be configured to detect branch instructions and to store branch prediction information corresponding to the branch instructions into the branch prediction unit. However, *Narayan* provides no further detail on the nature of the branch prediction information or how it is used, and in particular, states nothing about the branch prediction information indicating *Narayan*'s branch prediction unit predicted that a byte is an opcode byte of an instruction. See col. 6, lines 54-58.

With respect to claim 31, the Examiner stated that *Narayan* teaches an instruction buffer comprising an indicator associated with each byte of each of the instructions stored therein, wherein the indicator has a true value if the BTAC predicts that the byte is an opcode byte. Applicant respectfully disagrees. As discussed in the previous paragraph, Applicant can find no teaching in *Narayan* of a instruction buffer having an indicator associated with each byte of each of the instructions stored in the instruction buffer, wherein the indicator has a true value if the branch target address cache predicts that the byte is an opcode byte of one of the instructions, which is a limitation recited by claim 31. For these reasons, Applicant respectfully requests that the Examiner withdraw his rejection to claim 31.

With respect to claims 43-49, these claims depend from independent claim 31, and add further limitations that are not obviated by *Narayan* in view of *Hoyt*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 43-49.

The Examiner rejected claims 34-36, 50-55, 59, and 61-65 under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., U.S. Patent No. 5,850,543 (hereinafter *Shiell*) in view of Roberts et al., U.S. Patent No. 5,752,069 (hereinafter *Roberts*). Furthermore, the Examiner rejected claims 37-38 under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., U.S. Patent No. 5,850,543 (hereinafter *Shiell*) in view of Roberts et al., U.S. Patent No. 5,752,069 (hereinafter *Roberts*) and further in view of *Narayan* and *Hoyt*. Applicant respectfully traverses the Examiner's rejections with respect to amended claim 34 and its dependent claims.

Claim 34 has been amended to include the limitations of now canceled claim 37. Applicant respectfully asserts for the reasons discussed above with respect to claim 31, *Shiell* in view of *Roberts* in view of *Narayan* in view of *Hoyt* does not obviate amended claim 34.

With respect to claims 35-36 and 38, these claims depend from amended independent claim 34, and add further limitations that are not obviated by *Shiell* in view of *Roberts* in

view of *Narayan* in view of *Hoyt*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 35-36 and 38.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 31, 34-36, 38 and 43-49 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

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Respectfully submitted,

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